as the signal frequency increases. Notice that the level of THD+N at 20kHz is well below the rated 0.1% THD+N value; a standard for most consumer applications.

SPiKe Protection

The SPiKe Protection system requires additional explanation. Figure 27 is a simplified version of the advanced circuit that provides this protection.

The overvoltage clamping circuit operates by turning off the converse output transistor after sensing that the output has risen above the supply rail, thus protecting the output stage from exceeding its breakdown voltage. Once the opposite output transistor is protected, the operating transistor is protected by limiting the level of output voltage swing.

An undervoltage protection circuit eliminates turn-on/off pops at the output by disabling the internal biasing circuit until the supply voltage rails are greater than 18V. This feature eliminates the worry of output stage instabilities upon power-down.

The mute function works by turning off all the device's biasing circuits, placing the output stage in a high impedance state, and eliminating any output pops.

The internal current limiting circuit pulls base current away from the drive transistor after sensing that the instantaneous output current is too large.

The SPiKe protection circuit continuously monitors the output drive transistor's condition until an SOA violation occurs, at which time, the drive current of the transistor is internally reduced, bringing the operation of the device back into the safe operating area.

In addition, a thermal shutdown circuit monitors die temperature to protect the output transistors from thermal runaway.

Because these high-power, monolithic audio power amplifiers are inherently and dynamically protected against SOA violations, the audio designer can now easily design compact high-performance audio amplification systems at a reasonable cost.

Op Amp Test Circuits

John Christensen

Often, questions arise about operational amplifiers but none so regularly as, "how is such-and-such parameter tested?" This article is the first of a four-part series that revisits the whys and hows of operational amplifier testing. We will dust-off some methods that have been around our industry for some time, as well as address some issues that arise in part due to technology's advancement.

Offset Voltage (V_{os})

The first test, and one of the easiest, measures offset voltage. This voltage appears to be in series with the non-inverting input of an op amp when there is no outside signal applied. The cause of this voltage is primarily caused by manufacturing differences within the op amp input stage. As these errors from absolute perfection can go either way, V_{os} can be ± from zero.

Ideally, V_{os} could be measured by connecting a low, variable voltage source between the inputs of the op amp and adjusting it until the output is zero. (This assumes two equal and opposite polarity supplies, +Vs and -Vs are powering the op amp.) The value of the voltage at the input would be measured. This value is equal and opposite to the offset voltage. There are several serious problems with this method that make it impractical. First, the typical open loop gain of a modern op amp is usually around one million. To keep the output reasonably near zero, the input voltage must be adjusted to be equal to V_{os} within a microvolt or so. Even measuring this low voltage on an automated test system would prove very difficult.

Using the op amp to measure its own V_{os} and amplify the V_{os} by a large value will make the whole job quite easy.

In Figure 28, the device under test (DUT) is connected as an inverting amplifier with a closed-loop gain of 1,000.

Any apparent voltage between the inputs will be amplified by the op amp and cause the output to change until the inputs appear to have zero voltage between them. This causes a voltage at the output to be equal and opposite to the Vos times the division ratio of Rf/Rin. This now makes the adjustment of the input

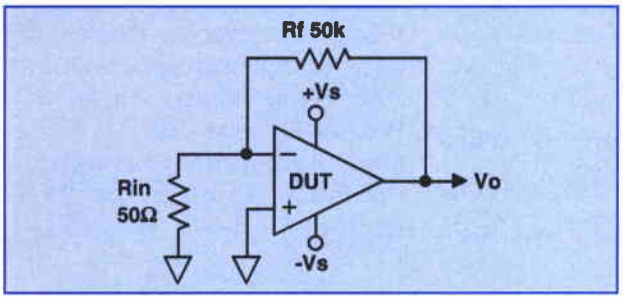

Figure 28: V_{os} Measurement

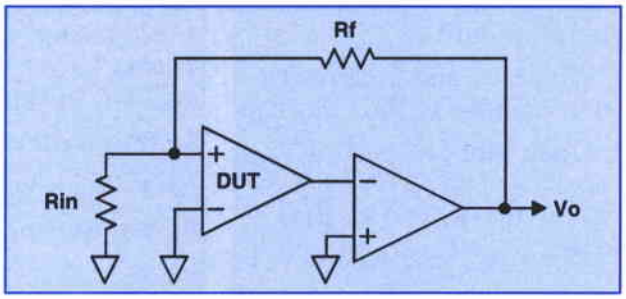

Figure 29: Second Op Amp Adds Buffering

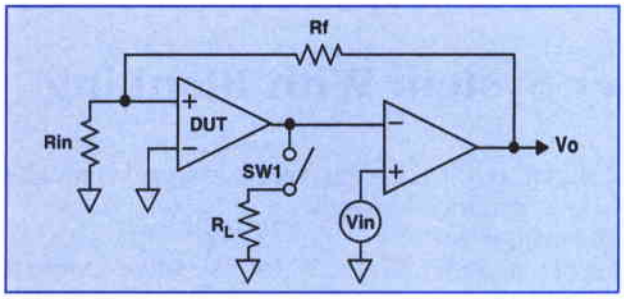

Figure 30: Open Loop Voltage Gain

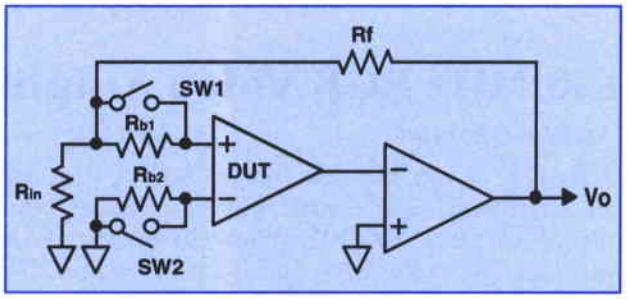

Figure 31: Input Bias Current Measurement

completely automatic as well as providing a large, easily measured output of 1V for each mV of V_{os}.

Test circuits often include a 50Ω resistor between the non-inverting input of the DUT and ground. This is done to cancel the effect of the input bias current being dropped across R_{in}. Usually, the only contribution of this additional resistor is a bit of noise, as the error from a 10nA input current is only 0.5µV in the V_{os} measurement.

When a full sequence of tests is to be performed on the same DUT, a second op amp is often added to the loop as shown in Figure 29. In the V_{os} test alone, the only result is to remove the effect of loading the output of the DUT with R_f. Notice also the necessary reversal of the DUT inputs to maintain the correct feedback phase after going through the second op amp.

More on the reason for this second op amp later in this series.

Open Loop Voltage Gain (Avol)

Open loop or large-signal voltage gain is a test that can use almost the same setup as the V_{os} test (Figure 30). The only difference is that a known signal, V_{in}, is injected into the non-inverting input of the second op amp. This forces the DUT output to swing to the same value. The voltage that appears at V_o is R_f/R_{in} times the voltage required at the input of the DUT to make its output swing by V_{in}.

Using values of 50Ω for R_{in} and 50kΩ for R_f, V_o will be 1000 times the voltage at the input to the DUT.

The procedure is as follows:

1. With V_{in} = 0, measure and record V_{o1}. (This is 1000 V_{os})
2. Change V_{in} to a positive value, i.e., +10V. (V_{in1}) Measure and record V_{o2}.
3. Change V_{in} to a negative value, i.e., -10V. (V_{in2}) Measure and record V_{o3}.
4. Subtract V_{o2} from V_{o3} to get ΔV_o.
5. Calculate:

$$A_{vol} = \frac{(R_f/R_{in})(V_{in1} - V_{in2})}{\Delta V_o}$$

This is the average open loop gain between ±10V out. This is the most common method used to verify the data sheet A_{Vol} specification. The separate gains between 0 and +10V or 0 and -10V out can be calculated by using V_{o1} and V_{o2} or V_{o1} and V_{o3}. A_{Vol} is usually specified with the output of the op amp loaded. To make this test, close Sw1 with R_L equal to the specified load. A_{Vol} is commonly specified in V/mV where 1V/mV = an open loop gain of 1000.

Placing two switches, Sw1 and Sw2, and two resistors, R_{b1} and R_{b2}, to our test loop, allows us to measure input bias current (I_b) and input offset current (I_{os}) (Figure 31).

The procedure is:

1. With Sw1 and 2 closed, record V_{o1} (this is $V_{os} * (R_f/R_{in})$.

2. Open Sw1 and record V_{o2}. This is:
$(V_{os} \pm (I_{b+} * R_{b1})) * R_f/R_{in}$

3. Open Sw2 and record V_{o3}. This is:
$(V_{os} \pm (I_{os} * (R_{b1} + R_{b2})) * (R_f/R_{in}))$

4. Close Sw1 and record V_{o4}. This is:
$(V_{os} \pm (I_{b-} * R_{b2})) * (R_f/R_{in})$

Solving for the currents yields:

$I_{b+} = (V_{o2} - V_{o1})/((R_f/R_{in})(R_{b1}))$

$I_{b-} = (V_{o4} - V_{o1})/((R_f/R_{in})(R_{b2}))$

$I_{os} = (V_{o3} - V_{o1})/((R_f/R_{in})(R_{b1}+R_{b2}))$

The value of I_b on most data sheets is the average of the two, or $(I_{b+} + I_{b-})/2$.

We invite comments. Please write to us at: National Semiconductor, 2900 Semiconductor Drive, P.O. Box 58090, Santa Clara, CA 95052-8090, Attn: John Christensen, Principal Applications Engineer, M/S C2-505.

130 MHz RGB Video Amplifier System With Blanking

David Westerman

Designing a monitor has now become even easier with the release of the LM1205 from National. Its 130 MHz bandwidth makes this part an ideal choice for monitors with resolutions up to 1280 x 1024. Also, the LM1205 allows blanking at the CRT cathode. When the blanking pulse is applied to the LM1205, its output goes to less than 100 mV above ground, providing a "blacker than black" output. High voltage transistors required to perform blanking to the first grid of the CRT are no longer necessary.

Figure 32 is a block diagram of the green channel of the LM1205 along with the recommended external components. Pin numbers are circled and all external components are shown outside the dashed line. The other two video channels are identical to the green channel, only the numbers to the pins unique to each channel are different. The video signal is AC coupled through a 10µF capacitor to the input, pin 6. Internal to the LM1205 is a 2.8V reference, giving the input video a 2.8V offset. This voltage was selected to give the input video enough DC offset to guarantee that the lowest voltage of the video signal at pin 6 is far enough above ground to keep the LM1205 in the active region. The 200Ω resistor at the input is for ESD protection and current limiting during any voltage surge that may occur at the input, driving pin 6 above V_{CC}. The input video signal is buffered by -A1, an inverting amplifier. The output of -A1 goes to the contrast and drive attenuator sections.

Contrast and drive control sections are virtually identical. Both sections take a 0V to 4V input signal, with 4V giving the maximum gain for either the contrast or the drive. This is a high impedance input, allowing an easy interface to 5V DACs. You can also use 100kΩ potentiometers with no degradation in performance.

The contrast control section is common to all three channels. It converts the input voltage at pin 12 to a couple of internal DC voltages that control the gain of the contrast attenuator. A 4V control voltage causes no video signal attenuation. A 0.5V control voltage results in 35dB attenuation. Because internal control voltages are common to all three channels, crosstalk can occur. These voltages go to pins 1 and 2. Adding the RC network shown in the block diagram prevents crosstalk.

The 0V to 4V drive control signal is applied to pin 18. Each channel has its own drive section, therefore the crosstalk compensation needed for the contrast control voltages is not required for the drive control. Thus, there are no external pins for the drive control. The drive attenuator gives an attenuation range from 0dB to -6dB. A small gain adjustment range for the drive attenuator is desirable and intentionally designed because the drive is used only to balance the overall gain of each color channel, giving the correct color temperature on the CRT.

The output of the drive attenuator stage goes to A2, the amplifier in the DC restoration section. The video signal goes to the non-inverting input of A2. The inverting side of A2 goes to the output of gm1, the clamp comparator, and the clamp capacitor at pin 8. During the back porch period of the video signal a negative going clamp pulse from pin 14 is applied to the clamp comparator, turning on the comparator. This period is where the black level of the video signal at the output of the LM1205 is compared to the