Simple circuit lets you characterize JFETs

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When working with discrete JFETs, designers may need to accommodate a large variation in device parameters for a given transistor type. A square-law **equation** is usually used as an approximate model for the drain-current characteristic of the JFET: $I_D=\beta(V_{GS}-V_P)^2$, where I_D is the drain current, V_{GS} is the gate-to-source voltage, β is the transconductance parameter, and V_P is the gate pinch-off voltage. With this approximation, the following **equation** yields the zero-bias drain current at a gate-to-source voltage of 0V: $I_{DSS}=\beta V_P^2$, where I_{DSS} is the zero-bias drain current.

Figure 1 is a plot of this characteristic for N-channel JFETs showing the variation possible in a collection of devices. For example, the 2N4416A's data sheet lists a pinch-off voltage of −2.5 to −6V, and the zero-bias drain current can range from 5 to 15 mA. You can observe the correlation between these two parameters across a sample of devices. The outer curves in the plot represent these extreme cases, and the center curve represents perhaps a typical case of a pinch-off voltage of −4V and a zero-bias drain current of 8 mA.

Although you can design around a certain amount of device variation for a mass-produced circuit, you sometimes need a tool to quickly characterize an assortment of discrete devices. This tool allows you to select a device that will optimize one circuit or perhaps to find a pair of devices with parameters that match reasonably well.

Figure 2 shows a simple test circuit for this purpose. Although the **figure** shows the JFET as an N-channel device, the JFET DUT (device under test) may be of either polarity, as selected by switch S_1.

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An external voltmeter connects to the terminals on the right. Switch S_2 selects two distinct measurement modes—one for the pinch-off voltage and another for the zero-bias drain current. In the pinch-off-voltage mode, the external voltmeter directly reads the pinch-off voltage; in the zero-bias-drain-current mode, the measured voltage is the zero-bias drain current across an apparent resistance of 100Ω.

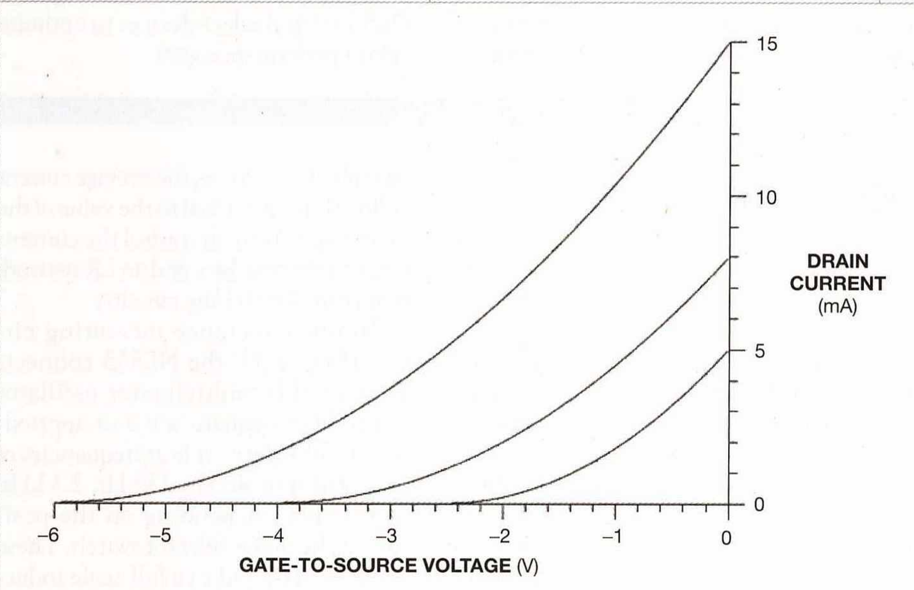

Figure 1 N-channel JFETs' I_D versus V_{GS} can vary widely among devices.

With S_2 in the pinch-off-voltage mode, R_1 allows a few microamps of drain current to flow in the JFET under test, and the source voltage is a close approximation of the negative of the pinch-off voltage. The op amp acts as a unity-gain buffer, with negative feedback through R_3, so you can directly read the negative of the pinch-off voltage with the external voltmeter.

In the zero-bias-drain-current mode, however, the resistance from JFET source to ground is only 10Ω, so the drain current is a close approximation of the zero-bias drain current. The op amp's feedback also switches to a gain-of-10 configuration, with the inclusion of R_4 and R_5 in the feedback-voltage divider. This gain allows the voltmeter to easily read the small volt-

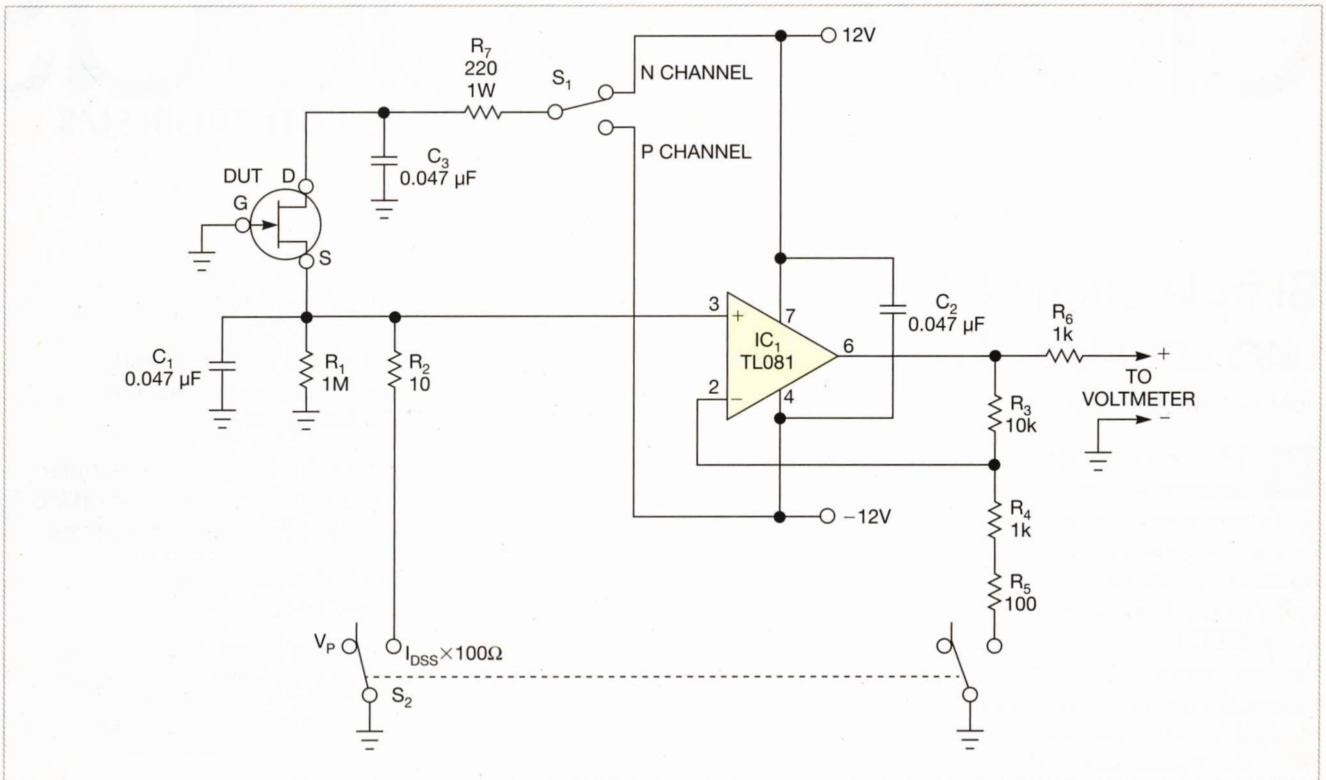

Figure 2 Selecting between the DUT's source resistors, R_1 and R_2, allows you to measure the pinch-off voltage and zero-bias drain current.

age across R_2, with the resulting reading being the zero-bias drain current times 100Ω. For example, if the voltmeter reads 1V, this voltage corresponds to a zero-bias drain current of 10 mA.

For an N-channel device, both voltage readings are positive; for a P-channel device, the circuit functions in the same manner except that the voltage readings are negative. If you wire the test JFET to this circuit with test leads and clips, each with some parasitic series inductance, you may need to add C_1 to suppress any tendency for high-frequency oscillation. R_6 isolates the op-amp feedback loop from any parasitic capacitance in the voltmeter and its leads, preserving the loop stability. R_7 protects against accidental shorts, and you can replace R_4 and R_5 with one 1.1-kΩ resistor. You are more likely to have on hand resistors with the values in the **figure**, however.

By clipping in samples from a collection of JFETs and throwing a switch, you can very quickly find the two parameters that determine where each JFET's characteristic falls in the range that **Figure 1** illustrates and select devices to optimize circuit performance. EDN

Use a transistor and an ammeter to measure inductance

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Bipolar junction transistors transfer a current from a lower-resistance emitter to a higher-resistance collector. You can use this property to measure inductance by connecting a series inductance/resistance circuit in the emitter and biasing on the transistor long enough for the current to reach a maximum value that is at least five LR time constants. When the transistor's off time is equal to its on time but is still biased by a silicon diode, the LR current decays exponentially toward 0A. Using the transistor's current-source property, you can measure this current without hindering the decay process in the LR circuit.

The transient analysis of an LR circuit shows that if, during the off time, the LR circuit's current reduces to a sufficiently low value, say 5% or less, then, for the on time plus the off time, the average current is directly proportional to the value of the inductance. You can control the currents through the transistor and an LR network using timed switching circuitry.

In an inductance-measuring circuit (**Figure 1**), the NE555 connects as an astable multivibrator oscillator to produce a square wave of approximately 50% duty cycle at frequencies of approximately 46 Hz, 230 Hz, 2.3 kHz, and 23 kHz, depending on the position of the range-selector switch. These values correspond to a full-scale inductance-measurement range as high as 2.5H, 500 mH, 50 mH, and 5 mH. This